REALTEK RTL8305SB DESIGN AND LAYOUT GUIDE

1. Introduction

This document provides detailed design and layout guidelines to achieve the best performance for implementing a 2-layer board design with the RTL8305SB 5 ports single chip switch.

The RTL8305SB is a Fast Ethernet switch, which integrates memory, five MACs, and five physical layer transceivers for 10Base-T and 100Base-TX operation into a single chip. To benefit BOM costs, one external PNP transistor is used to generate a 2.5V power source. Care needs to be taken, however, to prevent signals from cross-talk and interference due to the small package, and most importantly, to support a stable 2.5V power plane which determines the performance of data recovery and transmit jitter. The fifth port (port 4) supports an external MAC interface, which can be set to PHY mode MII, PHY mode SNI, or MAC mode MII to work with a routing engine, HomePNA or VDSL transceiver. The MII interface layout is also an important part in the system PCB design.

2. General Design and Layout Guide

In order to achieve maximum performance using the RTL8305SB, good design attention is required throughout the design and layout process. The following are some suggestions on recommendations to implement a high performance system.

General Guidelines

- Provide a good power source, minimizing noise from switching power supply circuits (<100mV).
- Verify the qualities of critical components such as clock source and transformer to meet application requirements.
- Keep power and ground noise levels below 100mV.
- Use bulk capacitors (4.7µF-10µF) between the power and ground planes.
- Use 0.1µF de-coupling capacitors to reduce high-frequency noise on the power and ground planes.
- Keep de-coupling capacitors as close as possible to the RTL8305SB chip.

Differential Signal Layout Guidelines

- Keep differential pairs as close as possible and route both traces as identically as possible.
- Avoid vias and layer changes if possible.
- Keep transmit and receive pairs away from each other. Run orthogonal or separate by a ground plane.

Clock Circuit

- Surround the clock by ground trace to minimize the high-frequency emission, if possible.
- Keep the crystal or oscillator as close to the RTL8305SB as possible.

2.5V Power

- Do not connect a bead directly between the collector of the PNP transistor and VDDAL. This will significantly affect the stability of the 2.5V power if such a bead is used.
- Use a bulk capacitor (4.7µF-10µF) between the collector of the PNP transistor and the ground plane.
- Do not use one PNP transistor for more than one RTL8305SB chip, even if the rating is enough. Use one transistor for each RTL8305SB chip.

Power Planes

- Divide the power plane into 2.5V digital, 2.5V analog, and 3.3V analog.
- Use 0.1μF decoupling capacitors and bulk capacitors between each power plane and the ground plane.
- Power line connects from source to the RTL8305SB pin should at least 10 mil width.

Ground Planes

- Keep the system ground region as one continuous, unbroken plane that extends from the primary side of the transformer to the rest of the board.
- Place a moat (gap) between the system ground and chassis ground.
- Ensure the chassis ground area is voided at some point such that no ground loop exists on the chassis ground area.

3. Transformer Application Circuit

The magnetic support Autoxover and with 1:1 turn ratio on both transmit and receive paths are valid for RTL8305SB. There are many venders improving their magnetic design to meet this requirement, and several are listed below.

Vendor	Quad	Single
Pulse	H1164	H1102
Magnetic 1	ML164	ML102
BothHand	40ST1041AX	TS6121C
Lankom	SQ-H48W	LF-H41S
GTS	FC-578S	FC618SM

Table 1, Reference Quad and Single transformer for RTL8305SB

10/100Base-T UTP application circuit with transformer is shown as the following two figures. The first is the circuit with Quad transformer and the second is the single transformer

- The center-tap of the primary side of the transformer ***should not*** be connected to ground with capacitors, because of the RTL8305SB's special design.
- The center-tap of the secondary side of the transformer ***should*** be connected to Chassis ground via a 50 pF capacitor.
- Center-tap of 50Ω termination-resister ***should*** be connected to ground with 0.1 uF capacitor.
- IBREF pin ***should*** connect to ground via a 2K Ω, 1% resister to bias the differential output voltage.

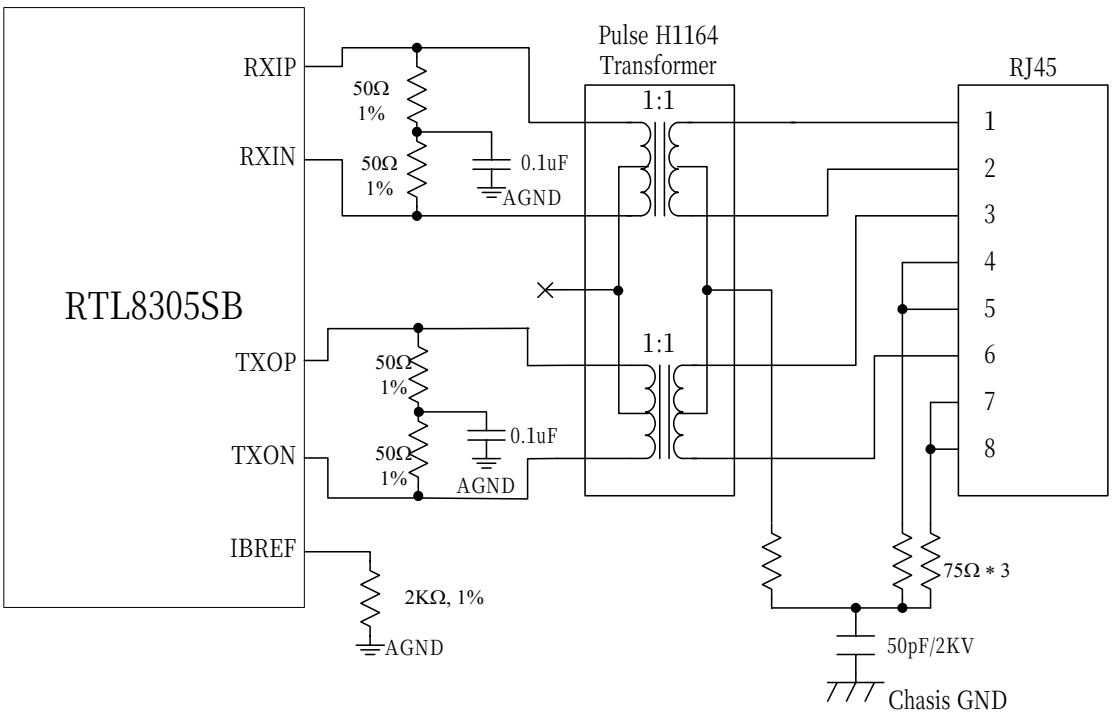


Figure 1, RTL8305SB UTP Application for Quad Transformer with Connected Central Tap

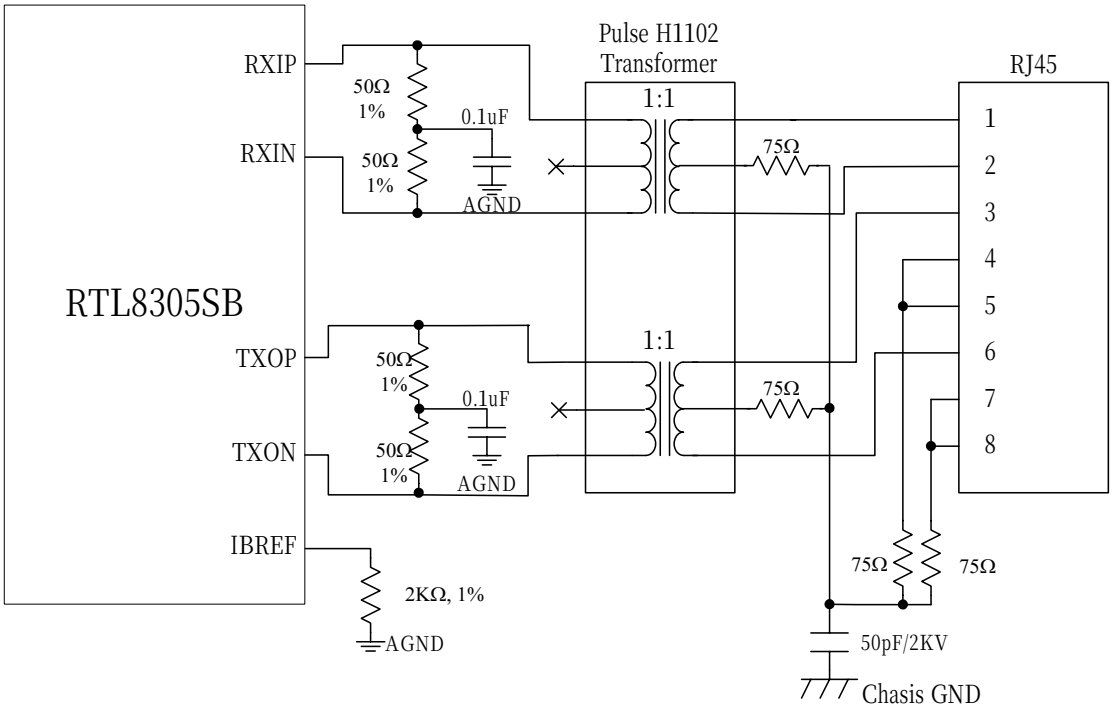


Figure 2, RTL8305SB UTP Application for Single Transformer with Connected Central Tap

4. 100Base-FX Application Circuit

All ports support 100Base-FX, which shares pins with UTP (TX+-/RX+-) and need no SD+- pins (Realtek patent). The 100Base-FX can be forced as half or full duplex with optional flow control ability. Hint: The 100Base-FX does not support Auto-Negotiation according to IEEE 802.3u. In order to operate correctly, both sides of the connection should set the same duplex and flow control ability. A scrambler is not needed in 100Base-FX. As compared to common 100Base-FX applications, the RTL8305SB lacks of a pair of differential SD (signal detect) signals to achieve link monitoring function (Realtek patent), which significantly reduces the pin count.

The following is an example for RTL8305SB connecting to 3.3V and 5V fiber transceiver application circuit with SIEMENS V23809-C8-C10 (3.3V~5V fiber transceiver, 1*9 SC Duplex Multimode 1300 nm LED Fast Ethernet/FDDI/ATM Optical Transceiver Module).

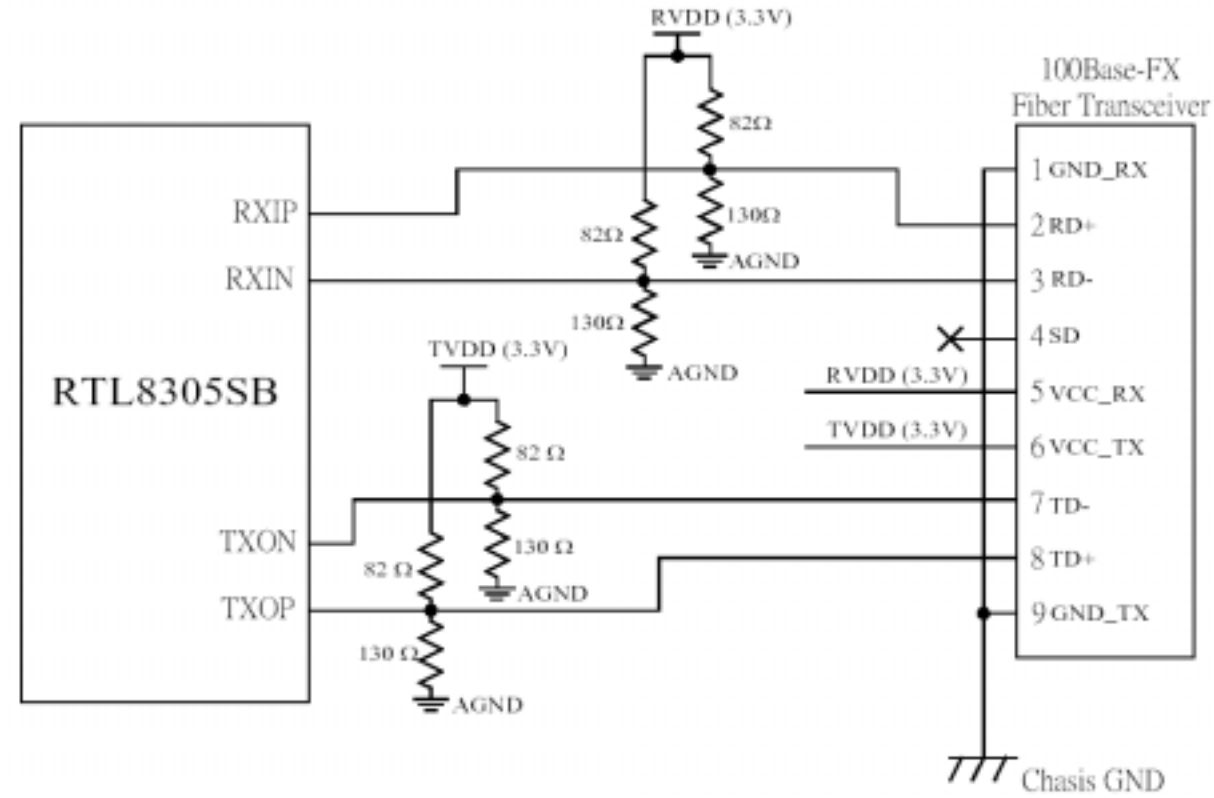


Figure 3, RTL8305SB 100Base-FX Application Circuit for 3.3V Fiber Transceiver

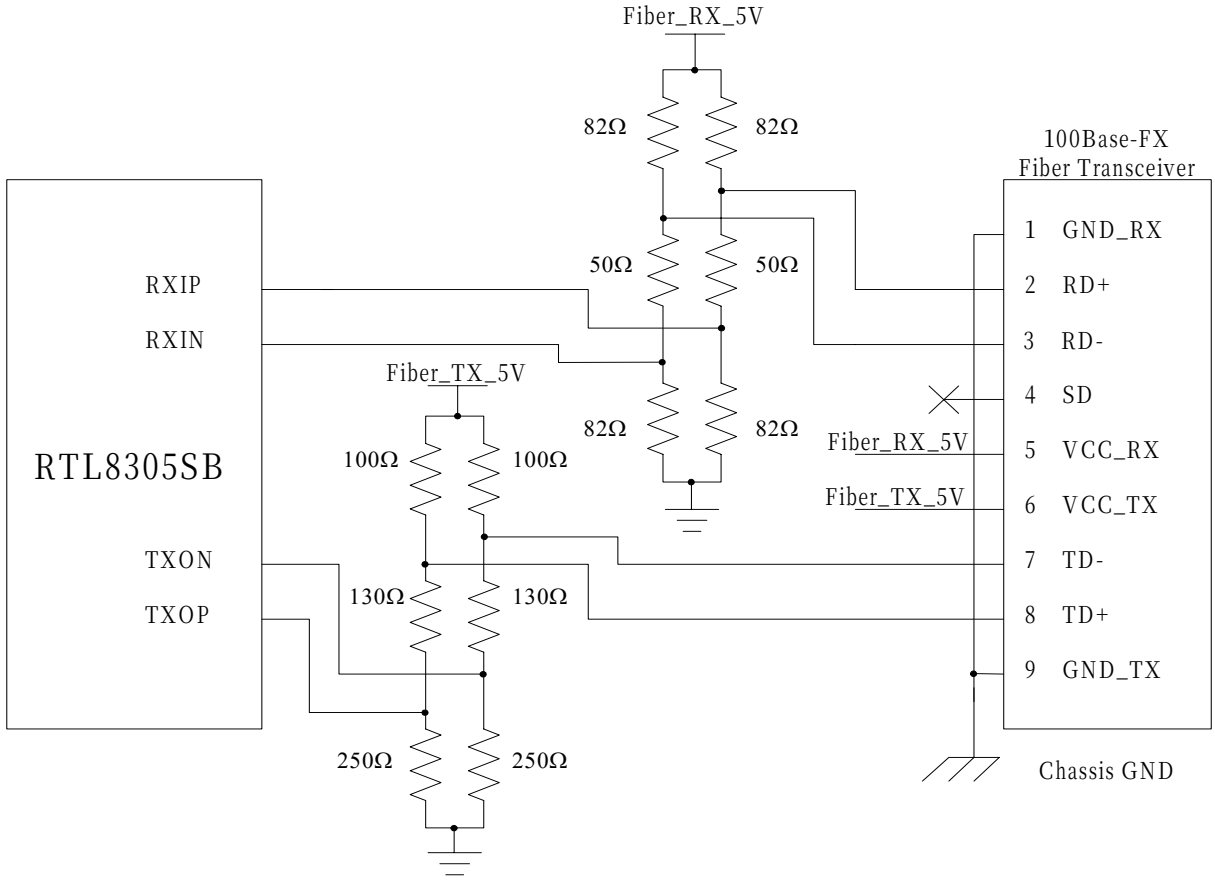


Figure 4, RTL8305SB 100Base-FX Application Circuit for 5V Fiber Transceiver

5. 2.5V Power Generation

The RTL8305SB uses a PNP transistor to generate 2.5V from the 3.3V power supply. This 2.5V provides for digital core and analog receive circuits. When designs require more than one RTL8305SB chip (a system greater than 8 ports), do not use one PNP transistor for all of the RTL8305SB chips even if the rating is sufficient. Use one PNP transistor for each RTL8305SB chip.

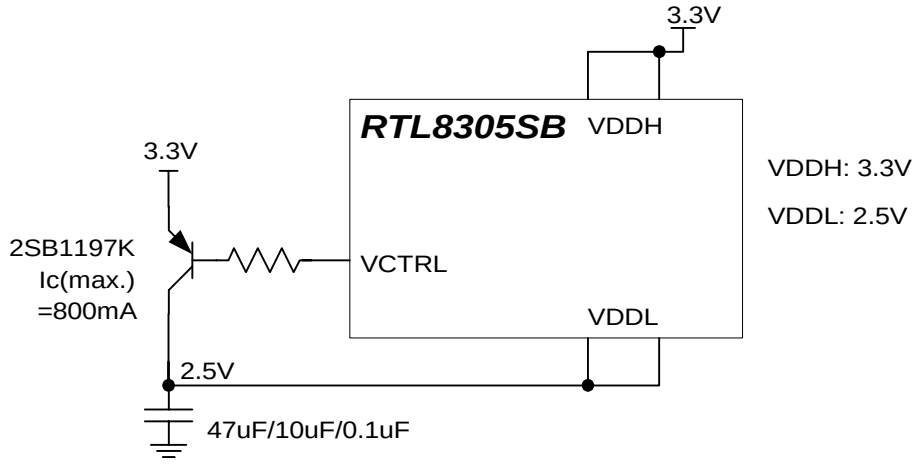


Figure 5, Using a PNP Transistor to Produce 2.5V

Use PNP transistor to transform 3.3V into 2.5V

Do not connect any beads directly between the collector of the PNP transistor and VDDAL. This will affect the stability of the 2.5V power significantly if a bead is used in this manner.

The power transistor is a 2SB1197K, and follows the following specifications.

Absolute maximum ratings (Ta=25°C)

Parameter	Symbol	Limits	Unit
Collector-base voltage	VCBO	-40	V
Collector-emitter voltage	VCEO	-32	V
Emitter-base voltage	VEBO	-5	V
Collector current	IC	-0.8	A(DC)
Collector power dissipation	PC	0.2	W
Junction temperature	Tj	150	°C
Storage temperature	Tstg	-55~+150	°C

Table 2, Specification of 2SB1197K PNP power transistor

For more information, refer to http://www.rohm.com

6. MII Interface Application Circuit

Operation mode of port4:

The fifth port (port 4) supports an external MAC interface which can be set to PHY mode MII, PHY mode SNI, or MAC mode MII to work with an external MAC of a routing engine, PHY of a HomePNA or other physical layer transceiver.

If the MAC part of Port4 connects with an external MAC, such as processor for a router application, it should act as a PHY. This is PHY mode MII or PHY mode SNI. In PHY mode MII or PHY mode SNI, Port4 uses the MAC part only, and provides an external MAC interface to connect MAC of external device. In order to connect both MACs, the MII of the switch MAC should be reversed into PHY mode.

If the MAC part of Port4 connects with an external PHY, such as a PHY for a HomePNA application, Port4 should act as MAC. This is MAC mode MII. In MAC mode MII, Port4 uses its MAC to connect external PHY and ignores the internal PHY part.

Port4 status pins:

When P4MODE[1:0]=11, Port4 can be either UTP or MAC mode MII. Port4 will automatically detect the link status of UTP from internal PHY and link status MAC mode MII from both TXC of external PHY and P4LNKSTA#. If both UTP and MII port are linked OK, UTP has higher priority and RTL8305SB will ignore the signal of MII port.

In UTP and FX mode, the internal PHY will provide the port status (Link/Speed/Duplex/Full Flow Control ability) in real time. In order to provide the initial configuration of Port4's PHY (UTP or FX mode), four pins (P4ANEG, P4Full, P4Spd100, P4EnFC) are used to strap upon reset. *Note: these 3 pins are changed as high active in order to provide dual function. For example: RTL8305SB=P4SpdSta/P4Spd100, RTL8305SB=P4SpdSta#.*

In the other three modes, four pins (P4LNKSTA#, P4SpdSta, P4DupSta, P4FLCTRL) are necessary in order to provides the port status to Port4's MAC in real time. That means that the external MAC or PHY should be forced to the same port status as Port4's MAC.

Related pins:

Pin **SEL_MIIMAC#** can be used to indicate MII MAC port active after reset for the sake of UTP/MII auto-detection. One 25MHz clock output (pin CK25MOUT) can be used as a clock source of the underlying HomePNA/other PHY physical devices. *Note: the output voltage is 2.5V for RTL8305SB but is 3.3V for RTL8305S.*

PHY mode MII/PHY mode SNI:

In routing application, RTL8305SB cooperates with a routing engine to communicate with WAN (Wide Area Network) through MII/SNI. In such application, P4LNKSTA# =0 and P4MODE[1] is pulled low upon reset. P4MODE[0] determines whether MII or SNI mode is selected.

In MII (nibble) mode (P4MODE[0]=1), P4SPDSTA=1 results in MII operating at 100Mbps with MTXC and MRXC runs at 25MHz; however, P4SPDSTA=0 leads to MII operating at 10Mbps with MTXC and MRXC runs at 2.5MHz.

In SNI (serial) mode (P4MODE[0]=0), P4SPDSTA takes no effect and should be pull-down. SNI mode operates at 10Mbps only, with MTXC and MRXC running at 10MHz. In SNI mode, RTL8305SB does not loopback RXDV signal as response to TXEN and does not support heart-beat function. (asserting COL signal for each complete of TXEN signal).

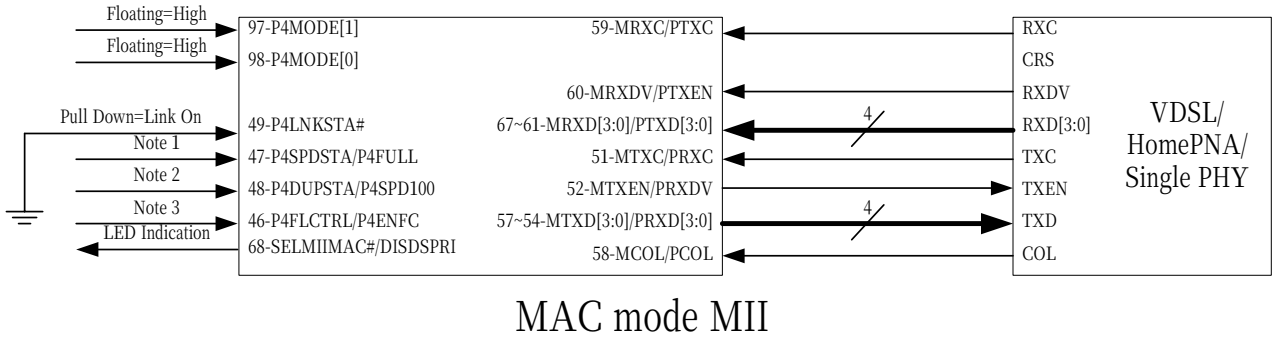
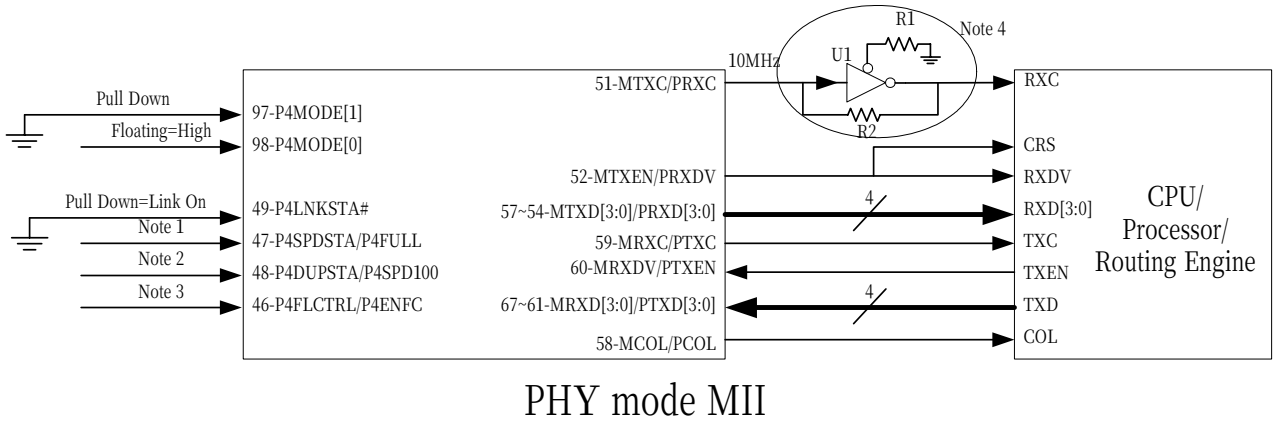
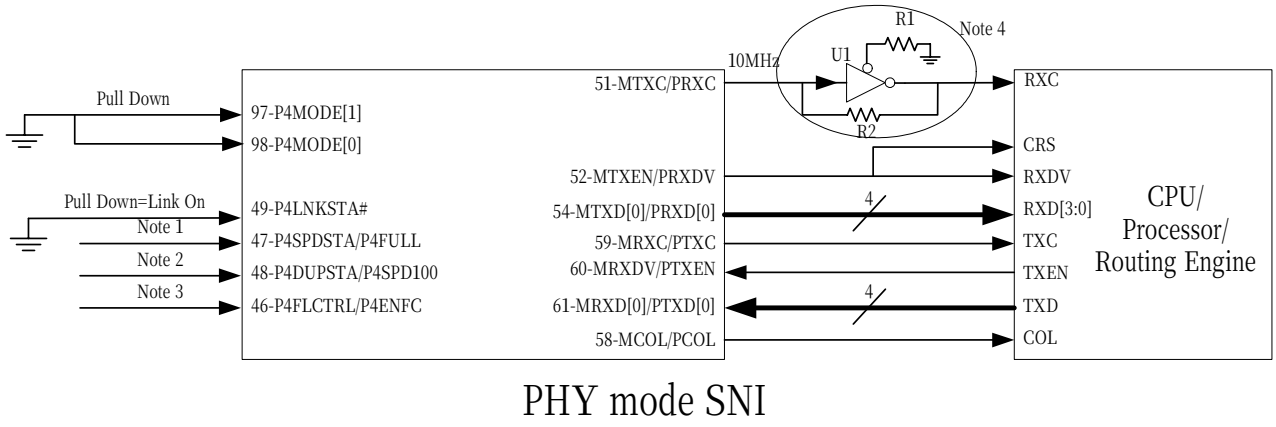


Figure 6, MAC mode MII Interface Application Circuit



PHY mode MII

Figure 7, PHY mode MII Interface Application Circuit



PHY mode SNI

Figure 8, PHY mode SNI Interface Application Circuit

Note 1: Pull high or floating means to set the speed as 100Mbps and pull down means to set the speed as 10Mbps.
Note 2: Pull high or floating means to set as full duplex and pull down means to set as half duplex.
Note 3: Pull high or floating means to enable flow control or backpressure and pull down means to disable flow control or backpressure.
Note 4: R1 is used to enable/disable the single logic gate, R2 is used to bypass the single logic gate, and U1 could be optional selected as 74LVC1G04 or 74LVC1G125 to fine tune the timing of MII interface trace, if the layout path is longer than 10 cm.

7. LED Application Circuit

The RTL8305SB supports four parallel LEDs for each port, and two special LEDs (SELMIIMAC# and LOOPLED#). Each port has four LED indicator pins. Each pin may have different indicator meaning set by pins LEDMode[1:0], refer to the pin descriptions for details. Upon reset, the RTL8305SB supports diagnostics of chip reset and LED functions by blinking all LEDs once for 320ms. This function can be disabled by asserting EN_RST_LINK to 0. LED_BLINK_TIME determines LED blinking period for activity and collision, with 1 = 43ms and 0 = 120ms. The parallel LEDs corresponding to port 4 can be three-stated (disable LED functions) for MII port application by setting ENP4LED in EEPROM as 0. In UTP application, this bit should be 1 to drive LEDs of port 4.

All LED pins are dual function pins: input operation for configuration upon reset, and output operation for LED after reset. If the pin input is floating upon reset, the pin output is active low after reset. Otherwise, if the pin input is pulled down upon reset, the pin output is active high after reset. Exception: Bi-color Link/Act mode of pin LED_ADD[4:0] when LEDMode[1:0]=10. Below shows an example circuits for LEDs. The typical values for pull-down resistors are 10K Ω.

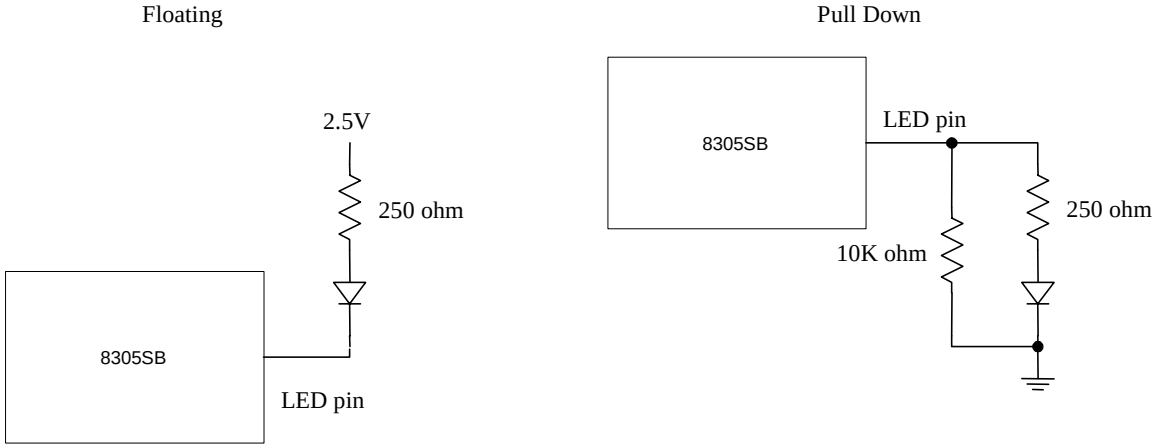


Figure 9, Floating and Pull-Down of LED pins

For two pin Bi-color LED mode (LEDMode[1:0]=10), Bi-color Link/Act (pin LED_ADD) and Spd (pin LED_SPD) can be used for one Bi-color LED package, which is a single LED package with two LEDs connected in parallel with opposite polarity. When LEDMode[1:0]=10, the active status of LED_ADD is opposite with LED_SPD, does nothing with input upon reset.

Indication	**Bi-Color state**	**Spd:Input=Floating, Active Low.** **Bi-color Link/Act:** the active status of LED_ADD is opposite with LED_SPD, does nothing with input upon reset.		**Spd:Input=Pull-down, Active High.** **Bi-color Link/Act:** the active status of LED_ADD is opposite with LED_SPD, does nothing with input upon reset.	
		Spd	**Link/Act**	**Spd**	**Link/Act**
No Link	Both Off	1	1	0	0
100M Link	Green On	0	1	1	0
10M Link	Yellow On	1	0	0	1
100M Act	Green Flash	0	Flash	1	Flash
10M Act	Yellow Flash	1	Flash	0	Flash

Table 3: Truth table of Spd and Bi-color Link/Act

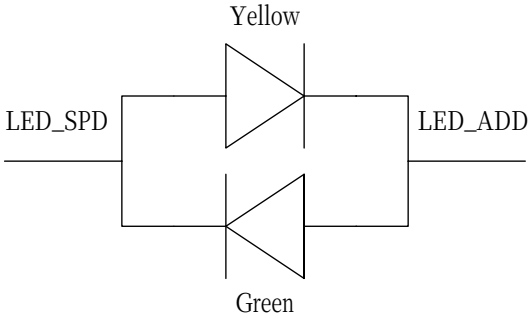


Figure 10: Two pin Bi-color LED for SPD floating or Pull-high

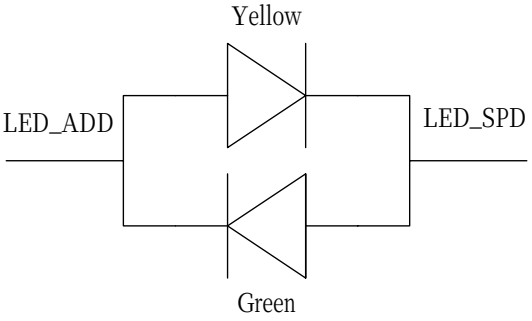


Figure 11: Two pins Bi-color LED for SPD Pull-down

8. Document Revision History

Revision	Release Date	Summary
1.0	2002/04/09	First release.

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